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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,443	12/30/2003	Eric Neyret	4717-8300	1763

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EXAMINER	
DANG, PHUC T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/750,443	NEYRET ET AL.	
	Examiner	Art Unit	
	PHUC T. DANG	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on April 13, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6 and 15-22* is/are rejected.

7)☒ Claim(s) *2,7-14 and 23-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's argument filed on April 13, 2005 with respect to claims 1-20 and newly added claims 21-26 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al., hereinafter "Kobayashi" (U.S. Patent No. 6,809,015 B2).

Kobayashi discloses a method for reducing by roughness of a free surface of a semiconductor wafer which comprises applying an annealing process under a pure argon atmosphere for a time sufficient to umiformly heat and smooth the free surface of the wafer [col. 7, lines 66-col. 8, lines 11].

Kobayashi discloses the features of the claimed invention as discussed above, but does not disclose a rapid thermal annealing step in the process.

However, a rapid thermal annealing step in the process is considered to be obvious in design of choice, since this step can be used after heating the surface of the electronic semiconductor device. Thus, it would have been obvious to one having ordinary skilled in the art at the time the

invention was made to modify the above teaching with the rapid thermal annealing process for a purpose of obtaining the wafer surface roughness with high productivity.

Regarding claim 15, Kobayashi discloses a step of forming a silicon-on-insulator structure having a free surface with enhanced smoothness [col. 8, lines 12-25].

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Falster (U.S. Patent No. 5,403,406).

Kobayashi discloses the features of the claimed invention as discussed above, but does not disclose a step comprising polishing the wafer after the rapid thermal annealing.

Falster, however, discloses a step comprising polishing the wafer after the rapid thermal annealing [col. 5, lines 12-16].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Kobayashi to Falster discussed above such that the step comprising polishing the wafer after the rapid thermal annealing for a purpose of reducing the roughness on the free surface.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Zhong et al., hereinafter "Zhong" (U.S. Patent No. 5,966,625).

Kobayashi discloses the features of the claimed invention as discussed above, but does not disclose a step comprising implementing at least one sacrificial oxidation stage to reduce slip lines in the free surface of the wafer.

Zhong, however, discloses a step comprising implementing at least one sacrificial oxidation stage to reduce slip lines in the free surface of the wafer [col. 2, lines 16-20].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Kobayashi to Zhong discussed above such that the step comprising implementing at least one sacrificial oxidation stage to reduce slip lines in the free surface of the wafer for a purpose of reducing the roughness on the free surface.

5. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al., hereinafter "Yoshida" (U.S. Patent No. 6,577,386 B2).

Regarding claims 16, Yoshida discloses a method for reducing roughness of a free surface of a wafer of semiconductor material which comprises: .

placing a wafer into a chamber;

introducing an annealing atmosphere of pure argon into the chamber;

heating the chamber to increase temperature inside the chamber at a predetermined rate up to a treatment temperature;

maintaining the wafer in the chamber at the treatment temperature for a duration of a high-temperature dwell; and

cooling the wafer at a rate of several tenth of degrees Celsius per second [Figs. 2A-2C and col. 7, lines16-25].

Yoshida discloses all the features of the claimed invention as discussed above, but does not disclose annealing atmosphere of pure argon into the chamber at a predetermined pressure.

However, annealing atmosphere of pure argon into the chamber at a predetermined pressure is considered to be obvious in design of choice, since the pressure level can be varied in the chamber during in the process. Thus, it would have been obvious to one having ordinary skilled

in the art at the time the invention was made to modify the above teaching with the predetermined pressure for a purpose of obtaining the wafer surface roughness with high productivity.

6. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Pan et al., hereinafter "Pan" (U.S. Patent No. 6,589,609 B1).

Yoshida discloses the features of the claimed invention as discussed above, but does not disclose the cooling occurs by means of a flow air.

Pan, however, discloses the cooling occurs by means of a flow air [col. 8, lines 49-51].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching Yoshida to Pan discussed above such that the cooling occurs by means of a flow air for a purpose of reducing the roughness on the free surface.

7. Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Falster and further in view of Zhong.

Regarding claims 21-22, Yoshida discloses a method for reducing roughness on a free surface of a semiconductor wafer which comprises:

applying a rapid thermal annealing process under a pure argon atmosphere for a time sufficient to uniformly heat and smooth the free surface of the wafer [col. 7, lines 16-25].

Yoshida discloses the features of the claimed invention as discussed above, but does not disclose polishing the wafer; and implementing at least one additional treatment step comprises a sacrificial oxidation stage to reduce any remaining surface defects and enhance smoothness.

Falster, however, discloses polishing the wafer [col. 5, lines 12-16].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching Yoshida to Falster discussed above such that polishing the wafer for a purpose of reducing the roughness on the free surface.

Yoshida and Falster disclose the features of the claimed invention as discussed above, but does not disclose implementing at least one additional treatment step comprises a sacrificial oxidation stage to reduce any remaining surface defects and enhance smoothness.

Zhong, however, disclose implementing at least one additional treatment step comprises a sacrificial oxidation stage to reduce any remaining surface defects and enhance smoothness [col. 13, lines 9-24].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching Yoshida and Falster to Zhong discussed above such that implementing at least one additional treatment step comprises a sacrificial oxidation stage to reduce any remaining surface defects and enhance smoothness for a purpose of reducing the roughness on the free surface.

8. Kobayashi and Yoshida disclose the claimed invention except for the process parameters as claimed in claims 3-4 and 17-19. However, the selection of the claimed process parameters would have been obvious to one having ordinary skill in the art at the time the invention was made to improve a process for reducing roughness on a free surface of a semiconductor wafer, since it is well settle that when the general conditions of a claim are discloses in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Allowable Subject Matter

9. The following is a statement of reason for the indication of allowable subject matter:

Claims 2, 7-14 and 23-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

None of the Prior Art made of record discloses prior to conducting rapid thermal annealing, implanting atoms under a face of a donor substrate to form a zone of weakness, bonding a stiffening substrate to the face, and detaching the donor substrate along the zone of weakness to form the wafer including the stiffening substrate and a useful layer as cited in claim 2 and the sacrificial oxidation stage is conducted prior to the rapid thermal annealing as cited in claim 7 and the sacrificial oxidation stage is conducted after the rapid thermal annealing as cited in claim 8 and a first sacrificial oxidation stage is conducted prior to the rapid thermal annealing, and a second sacrificial oxidation stage is conducted after the rapid thermal annealing is followed by a first sacrificial oxidation stage, a polishing stage and a second sacrificial oxidation stage to further enhance free surface smoothness after the rapid thermal annealing as cited in claim 11 and further comprises another rapid thermal annealing stage under pure argon after polishing ti further enhance free surface smoothness as cited in claim 12 and further comprises conducting a first sacrificial oxidation stage prior to the polishing stage as cited in claim 13 and further comprises conducting a second sacrificial oxidation stage after the polishing stage as cited in claim 14 and the sacrificial oxidation stage is conducted after the rapid thermal annealing as cited in claim 23 and the sacrificial oxidation stage is conducted prior to the rapid thermal

annealing as cited in claim 24 and the at least one additional treatment step comprises a first sacrificial oxidation stage conducted prior to the rapid thermal annealing and a second sacrificial oxidation stage conducted after the rapid thermal annealing as cited in claim 25 and the at least one additional treatment step comprises conducting another rapid thermal annealing stage under pure argon after polishing to further enhance free surface smoothness as cited in claim 26.

Claim 10 is depend on claim 9, then, it also would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and After Final communications.

12. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Phuc T. Dang PD

Primary Examiner

Art Unit 2818